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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/660,254	GROEN ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) *2,7,17 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments (11/16/2007) have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the circuit portion chooses among the first recovered clock, the second recovered song and the reference clock..." must be shown or the feature(s) canceled from the claim(s). Fig. 5-7, only show clock based functionalities, the drawings do not show selection/choosing of clock signals as claimed by claims 1, 6, 10, 14, 19, 22, 23. Claim 8, recites: "wherein the logic provides each received input serial stream of the plurality of input serial data streams to the outgoing transmit block by choosing among each corresponding recovered clock of the plurality of corresponding clocks and said reference clock" these details are not shown in Figures 5-7

No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not

be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 6, recites: "wherein the first, second, and third clock based functionalities concurrently perform processing functions by choosing among the first recovered clock, the second recovered clock, and the reference clock, respectively" where it is understood that each of the clock based functionalities chooses among the three clocks, that contradicts earlier

limitations "the first circuitry provides the first received clock to a first clock based functionality", "providing a reference clock to a second clock based functionality;" the third circuitry provides the third received clock to a third clock based functionality." So although each clock based functionality receives a specific clock, it also chooses among all clock signals (that are supplied to other clock based functionalities)?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 6, 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Venkata et. al., (U.S.7,180,972).

With respect to claim 6, Venkata et. al., disclose: first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data (Fig. 2d, CDR block 130 output 134 is the recovered first clock , column 3; lines 21-22 first HSSC channel (high speed serial communication) column 3, lines 58-60); wherein the first circuitry provides the first recovered clock to a first clock based functionality (see Fig. 2d, mux 310, corresponds to a first based clock functionality); and second circuitry for generating and providing

a reference clock to a second clock based functionality (Fig. 2d and Fig. 2f (blocks 660, 710 used to generate clock 712 (corresponds to the reference clock), column 10, lines 1-5, 8-10, the reference clock is a slow speed parallel clock, the second clock based functionality is mux 320 as shown in Fig. 2d); third circuitry for receiving second serial data and recovering a second recovered clock based on the second serial data (the RX circuitry of channel 0, similar to the one shown in Fig. 2d, see column 3, lines 20-27, , wherein the third circuitry provides the second recovered clock to a third clock based functionality (the third clock based functionality is mux 330 on Fig. 2c, where one of its input is the recovered clock of channel 0, see column 10, lines 29-31, 40-41); and wherein the first, a second and third clock based functionalities concurrently perform processing functions by choosing among the first recovered clock, the second recovered clock, and the reference clock, respectively (the processing function of each of blocks 310, 320, 330 (muxes) is clock outputting/routing substantially concurrent (when the signal traces supplying the clocks signals is small)).

With respect to claim 10, Venkata et. al., disclose: at least one clock recovery circuitry coupled to receive a high data rate input data stream, wherein the clock recovery circuitry recovers a plurality of recovered clocks based on the high data rate input stream(Fig. 2d, signal 112 s the serial data input stream of one HSSC (column 1,lines 23-25) channel, see block 130 CDR, signal 134 is the recovered clock of the particular stream, N more channels with CDR circuits

outputting a plurality of recovered clocks, are also present , see column 3, lines 21-28, 58-60); and a programmable logic fabric portion wherein the programmable logic portion performs subsequent processing by choosing among the recovered clocks and a reference clock (Fig 2d, see circuit portion (corresponds to the claimed programmable logic fabric) comprising blocks 310, 150, 160, 170,180,190, column 3, lines 65-67 through column 4, lines 1-15 (programmable nature of the circuits) see also column 4, lines 36-37 circuitry 170 is also programmable, block 310 performs clock selection (has three inputs the channel 0 recovered clock, the particular channel recovered clock and a slow parallel clock(the reference clock), column 10, lines 1-2, 8-10, 20-31).

With respect to claim 11, Venkata et. al., disclose: wherein the high data rate input data stream is received according to a first protocol and is converted to a second protocol by the programmable logic fabric portion based on one of said plurality of recovered clocks (Fig. 2d, block 150 performs serial/parallel conversion using one recovered clock signal (the recovered clock of the particular channel)).

With respect to claim 12 Venkata et. al., disclose: transmit circuitry coupled to receive the converted high rate input data stream in the second protocol, (Fig. 2a, transmitter, receives parallel bit stream 264 from Fig. 2c, (connected to Fig. 2d) wherein the programmable logic fabric portion provides the converted high data rate input data stream in the second protocol based on

one of said plurality of the recovered clocks (Fig. 2c, function of 150 is based on one of the recovered clocks (134) and function of other second (parallel) domain processing blocks (170, 190...) based on (recovered) and reference clock selection (muxes 310, 320, 330)).

With respect to claim 13, Venkata et. al., disclose: wherein said at least one clock recovery circuitry comprises a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream (the entire quad circuitry comprises CDRs such as the one shown in Fig. 2d, column 3, lines 20-30).

With respect to claim 14, Venkata et. al., disclose: receiving a high data rate input data stream (Fig. 2d, signal received on RXP/N, column 1, lines 23-25, column 3, lines 21-22); recovering a first recovered clock based on the high data rate input data stream (Fig. 2d, CDR circuit 130, clock signal 134 of the channel); recovering a second recovered clock based on a transmitter clock (another channel receiver circuit such as the one shown in Fig2d, fro another channel, column 3, lines 20-27, and see that the clock recovery is based on a transmitter clock since the received signal is transmitted (Fig. 2a) based on a clock signal (TX-REF_CLK)); providing the first and second recovered clocks to a programmable logic fabric portion (Fig 2d, for channel other than channel 0, clock signals supplied to PLF comprising blocks 150-190, 310, 320, (supplied to the

muxes, see column 10, lines 20-31); and performing subsequent processing in the programmable logic fabric portion by choosing among the recovered (Fig. 2d, muxes 310, 320 choose among the supplied recovered clocks to processing blocks 170, 190) clocks, wherein the high data rate input data stream is received according to a first protocol (original signal was a serial signal) .

With respect to claim 15, see above rejection of claim 14.

With respect to claim 16, Venkata et. al., disclose: herein the high data rate input data stream is converted to a second protocol-based on the first recovered clock (Fig. 2d, see deserializer is clocked with first recovered clock, 134).

With respect to claim 18, Venkata et. al., disclose: further comprising transmitting the converted high data rate input data stream in the second protocol based on the second recovered clock (Fig. 2c, signal 264 when block 250 is bypassed , and when output of block 330 is the second recovered clock, signal 264 is supplied to Fig2a,Fi2b that perform a transmit operation).

With respect to method claims 19, 20 Venkata et. al., disclose: receiving a first serial bit stream and recovering a first recovered clock from the first serial bit stream (Fig. 2d, Channel 0, CDR 130, recovered clock 134, column 1, lines 23-25, column 3, lines 20-29, 58-60, see received signal 112 in Fig. 2d, column 9,

lines 64-65 the master channel); receiving a second serial bit stream and recovering a second recovered clock from the second serial bit stream (Fig 2d, for a channel other than the master channel (channel 1 for example), CDR 130, recovers the particular channel clock signal); providing the first and second recovered clocks and a reference clock to a circuit portion (Fig 2d, for channel 1, blocks 310, 170, 190, three clock inputs to mux 310, see column 10, lines 1-2, 8-11, the reference clock signal, and lines 29-31); and within the circuit portion, choosing among the first and second recovered clocks and the reference clock for subsequent processing (Fig. 2d, mux 310, selects among the three clock signals to supply to blocks 170,190).

With respect to claim 21, see above rejection of claim 19 and Venkata et. al., disclose: wherein the second serial bit stream is a transmit serial bit stream (the received serial streams on Fig.2d, were originally transmit streams, and the received bit stream are also routed (transmitted) to circuit portions of the receiver).

Method claim 22 is rejected based on a rationale similar to the one used to reject claim 6 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 4-6, 8-16, 18 -21, 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et. al., (U.S. 5,251,210) in view of Venkata et. al., (U.S. 7,180,972).

With respect to claim 1, Mann et. al., disclose: first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data (Fig. 7, see Channel 1,blocks 260, 250, see column 14, lines 28-39, for serial data streams see column 6, lines 39-43); a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data (Fig. 7, see Channel 2 blocks 260 and 250); wherein the transceiver provides the first recovered clock, the second recovered clock, the first serial data and the second serial data to a circuit portion of the transceiver (see column 1, lines 9-11, transmitting/receiving communication system (transceiver) and Fig. 7 (the receiver side), see circuit portion including block 240, fifos 210, (and blocks to the right of the fifos, see column 13, lines 54-67, column 14,lines 1-15)

Mann et. al., do not expressly teach: the transceiver provides a reference clock to a circuit portion of the transceiver; and wherein the circuit portion

chooses among the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first serial data and the second serial data;

In the same field of endeavor Venkata et. al., disclose: a circuit portion chooses among a first recovered clock, a second recovered clock, and a reference clock for subsequent processing of one a first data and a second data (Fig. 2d, muxes 310-320 and block 190 "de-skewing FIFO", of a first channel data, muxes select among a master channel recovered clock, the particular channel recovered clock, and a reference clock, see column 10, lines 1-10, 20-33)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et. al., based on the teachings of Venkata et. al., so that its capable of supporting different communication protocols based on user selection (Venkata et. al., column 11, 22-33)

With respect to claim 4, Mann et. al., disclose: wherein the first serial data is an receive serial bit stream (see column 3, lines 63-65 description of Fig. 7, and column 6, lines 39-43 where the first serial data of Fig. 7 (Channel 1 RxDATA) is a receive serial bit stream).

With respect to claim 5, Mann et. al., disclose: wherein the circuit portion comprises a portion of a programmable logic fabric (Fig. 7, block 240

"Reassembly Control Logic", see column 16, lines 39-44, the operation of block 240 implemented by a microprocessor or custom logic (any one of these corresponds to the claimed programmable logic fabric)).

With respect to claim 6 (as best understood), Mann et. al., disclose: first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data (Fig. 7, Channel 1, RxDATA blocks 260 and 250, column 14, lines 28-33, and column 6, lines 39-43 see serial data streams) wherein the first circuitry provides the first recovered clock to a first clock based functionality (Fig. 7, recovered clock CLK of Channel 1 is supplied to clock based functionality comprising blocks FIFO 210 (of Channel 1) blocks 220, 240); and second circuitry for generating and providing a reference clock to a second clock based functionality (Fig. 7, Channel 2, RxDATA blocks 260 and 250, column 14, lines 28-33, second clock based functionality includes FIDO 210 of channel 2, blocks 240, 250 column 6, lines 39-43 see serial data streams, and with respect to the "reference" clock signal (which is a recovered clock as shown in Fig. 7) see Applicant's own disclosure middle of paragraph [0054] "Generally, a transmit reference clock is merely a clock, perhaps a recovered clock"); third circuitry for receiving second serial data and recovering a second recovered clock based on the serial data (Fig. 7, Channel 3 (not shown), RxDATA blocks 260 and 250, column 14, lines 28-33, and column 6, lines 39-43 see serial data streams), wherein the third circuitry provides the second recovered clock to a third clock based functionality (Fig. 7, recovered clock CLK of Channel 3 is supplied to

clock based functionality comprising FIFO 210 blocks 220, 240 of Channel 3); and wherein the first and third clock based functionalities concurrently perform processing functions (Fig. 7, the function of the FIFOs and blocks 220 to supply data to combiner of each channel is understood to be (in theory) concurrent under control of block 240)

Mann et. al., do not expressly teach: and wherein the first, second and third clock based functionalities concurrently perform processing functions by choosing among the first recovered clock, the second recovered clock, and the reference clock, respectively.

In the same field of endeavor Venkata et. al., disclose: choosing among a plurality of clock signals (recovered and refrence) (muxes 310 (or 320, 330) select among a master channel recovered clock, the particular channel recovered clock, and a reference clock, see column 10, lines 1-10; 20-33)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et,. al., based on the teachings of Venkata et. al., so that the first, second and third clock based functionalities concurrently perform processing functions by choosing among the first recovered clock, the second recovered clock, and the reference clock, respectively, so that its capable of supporting different communication protocols based on user selection (Venkata et. al., column 11, 22-33)

With respect to claim 10, Mann et.al., disclose: at least one clock recovery circuitry coupled to receive a high data rate input data stream (Fig. 7, blocks 250 of the received data channels, see column 5, lines 52-53 the 1.536 megabit rate), wherein the clock recovery circuitry recovers a plurality of recovered clocks based on the high data rate input data stream (Fig. 7, function of CLK recovery blocks 250, see the plurality of CLKs); and a programmable logic fabric portion wherein the programmable logic fabric portion performs subsequent processing (Fig. 7, block 240, the recovered clock(s) are supplied to block 240, the CLKs are used for subsequent processing, see column 15, lines 58-65, and column 16, lines 39-44, the reassembly process implemented using a microprocessor or custom logic (any one of these corresponds to the claimed programmable logic fabric).

Mann et. al., do not expressly teach: subsequent processing by choosing among the recovered clocks and a reference clock.

In the same field of endeavor Venkata et. al., disclose: choosing among the recovered clocks and a reference clock (muxes 310 (or 320, 330) select among a master channel recovered clock, the particular channel recovered clock, and a reference clock, see column 10, lines 1-10, 20-33)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et,. al., based on the teachings of Venkata et. al., so that its capable of supporting different communication protocols based on user selection (Venkata et. al., column 11, 22-33)

With respect to claim 11, Mann et. al., disclose: wherein the high data rate input data stream is received according to a first protocol and is converted to a second protocol by the programmable logic fabric portion based on one of said plurality of recovered clocks (see Fig. 7, where the high data rate input data stream is a serial data stream (first protocol) and the RxDATA output (second protocol) is generated based on one of the plurality of recovered clocks, (used to perform realignment in block(s) 220).

With respect to claim 12, Mann et. al., disclose: further comprising transmit circuitry coupled to receive the converted high rate input data stream in the second protocol (Fig. 7, combiner (reassembling the data stream(s)) 230, that sends the RxDATA to the user interface), wherein the programmable logic fabric portion provides the converted high data rate input data stream in the second protocol based on one of said plurality of recovered clocks (see above rejection of claim 11).

With respect to claim 13, Mann et. al., disclose: wherein said at least one clock recovery circuitry comprises a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream (Fig. 7, Channel 2 processing of serial RxData, similar to the processing of Channel 1, serial data as explained in the rejection of claim 10 above).

With respect to claim 14, Mann et. al., disclose: receiving a high data rate input data stream; recovering a first recovered clock based on the high data rate input data stream (Fig. 7, Channel 1, blocks 260, 250 receiving Channel 1 data see column 5, lines 52-53 the 1.536 megabit rate); recovering a second recovered clock based on a transmitter clock (Fig. 7, second clock recovered from Channel 2 data, and see Fig. 5, transmitter uses a transmitter clock (block 110 to generate the Channel N data) providing the first and second recovered clocks to a programmable logic fabric portion (block 240 and FIFOs and blocks 220 comprise the programmable logic fabric, receives the recovered clocks from Channel 1 and Channel 2, (blocks 250), column 15, lines 58-65, column 16, lines 39-44); and performing subsequent processing in the programmable logic fabric portion (see column 15, lines 58-65, where the recovered CLK is used by block 240 to generate CLK1).

Mann et. al., do not expressly teach: by choosing among the recovered clocks.

In the same field of endeavor Venkata et. al., disclose: choosing among the recovered clocks (muxes 310 (or 320, 330) select among a master channel recovered clock, the particular channel recovered clock, and a reference clock, see column 10, lines 1-10, 20-33)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et,. al., based on the teachings of Venkata et. al., so that its capable of supporting different

communication protocols based on user selection (Venkata et. al., column 11, 22-33).

With respect to claim 15, Mann et. al., disclose: wherein the high data rate stream is received according to a first protocol (see column 6, lines 410-43, the received RxData of Channel 1 has serial format (first protocol), see column 6, lines 40-43).

With respect to claim 16, Mann et. al., disclose: wherein the high data rate input data stream is converted to a second protocol based on the first recovered clock (see Fig. 7, combiner 230, reassembles (combines) the high data rate stream (of Channel 1 for example) with other data streams, i.e. conversion to a second protocol (reassembled data)).

With respect to claim 18, Mann et. al., disclose: further comprising transmitting the converted data rate input data stream in the second protocol based on the second recovered clock (column 15, lines 58-67, the second recovered clock is used to generate CLK2 that is used in the FIFO of Channel 2 and the Alignment & Alignment monitor pattern detector 220, whose output is used in the conversion to the second protocol).

With respect to method claim 19, method claim 19 is rejected based on a rationale similar to the one used to reject apparatus claim 1above.

With respect to claims 20-21, Mann et.al., disclose: wherein the first serial bit stream is an receive serial bit stream (see column 6, lines 40-43); wherein the second serial bit stream is a transmit serial bit stream (again, column 6, lines 40-43, the RxxData serial channels, that were transmitted and realigned to be transmitted to the user interface).

With respect to method claim 22, method claim 22 is rejected based on a rationale similar to the one used to reject apparatus claim 6 above.

With respect to claim 23, Mann et. al., disclose: receiving a plurality of input data streams (Fig. 7, see plurality of receivers 260, receiving serial data from channels 1....N, column 6, lines 39-43, column 14, lines 16-21); recovering a corresponding plurality of clocks based on the plurality of input data streams (Fig. 7, blocks 250 of each channel, column 14, lines 28-33) ; determining at least one output port for providing outgoing data streams (Fig. 7, FIFOs 210 where every channel uses a specific (determined) FIFO therefore the channel 1 data are supplied to a corresponding channel 1 fifo (the determined output port)) ; and providing each input data stream of the plurality of input data streams to the at least one output port (see recovered data is supplied to its corresponding FIFO) ; wherein the at least one output port comprises a number of output ports

that corresponds to a number of input data streams of the plurality of input data streams (Fig. 7, see plurality of FIFOs 210 as many as the input data streams), and wherein the method further comprises determining, for each input data stream of the plurality of input data streams, an output port (Fig. 7, output ports of FIFOs 210) and providing each input data stream of the plurality of input data streams to the determined output ports (Fig. 7, each data stream is supplied to a specific FIFO).

Mann et. al., do not expressly teach: providing each input data stream of the plurality of data streams to the at least one output port by choosing among each corresponding recovered clock of the corresponding plurality of recovered clocks; based upon each corresponding chosen recovered clock of the corresponding plurality of recovered clocks.

In the same field of endeavor, Venkata et. al., disclose: choosing among a plurality of clock signals (muxes 310 (or 320, 330) select among a master channel recovered clock, the particular channel recovered clock, and a reference clock, see column 10, lines 1-10, 20-33)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et,. al., based on the teachings of Venkata et. al., so that its capable of supporting different communication protocols based on user selection (Venkata et. al., column 11, 22-33).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et. al., (U.S. 5,251,210) in view of Venkata et. al., (U.S. 7,180,972) as applied to claim 1 and further in view Tang et. al:, (U.S. 2002/0075981).

With respect to claim 3, With respect to claim 3, Mann et. al., disclose: further comprising circuitry (see Fig. 7, blocks 260, and 250 of Channel 2) for receiving second serial data and produces a second recovered clock from the second serial data (see Fig. 7. output of block 250, "CLK Recovery & Data Decoder", column 14, lines 27-28) in the transceiver provides the second serial data to the circuit portion and wherein the circuit portion (Fig. 7 (the receiver side), see circuit portion including block 240, fifos 210, (and blocks to the right of the fifos, see column 13, lines 54-67, column 14,lines 1-15, and the reference clock is clock RxCLK out of block 240, used to recombine the serial streams, see column 15, lines 34-39) uses one of the first recovered clock, the second recovered clock, and the reference clock for subsequent processing of one of the first and second serial stream data

Neither Mann et. al., nor Venkata et. al., expressly teach: delay locked loop circuitry. In the same field of endeavor (processing serial data and CDR) Tang et. al., disclose: delay locked loop circuitry (see Fig. 7, 703 clock recovery DLL, part of dual loop retimer see paragraphs [0036]-[0041]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et. al., based on the teachings of Tang et. al., so that the clock recovery circuit of Mann et. al., comprises a delay-locked loop circuit, (such as the clock recovery system of

Tang et. al.) that has minimum jitter generation and maximum jitter suppression (Tang et.al., [0013] and [0041]).

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et. al., (U.S. 5,251,210) in view of Venkata et. al., (U.S. 7,180,972) and McCormack et. al., (U.S. 6,463,109).

With respect to claim 8, Mann et. al., disclose: circuitry for receiving a plurality of input serial data streams (receiver of Fig. 7, see plurality of received serial streams on channels 1...N, column 6, lines 39-43 see serial data streams by blocks 260 and 250); clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams (Fig. 7, blocks 250 (for each received channel, column 14, lines 28-33,); and logic for providing at least one outgoing serial data stream to an outgoing transmit block data stream to a specific part of the circuit (Fig. 7, logic comprises FIFOs 210, blocks 220, block 240 that supply input serial streams to the combiner (outgoing transmit block))wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block (see Fig. 7, see that each received input serial stream is supplied to combiner 230)

Mann et. al., do not expressly teach: circuitry for providing a reference clock; (the) logic (for) selecting from the plurality of input serial data streams; by choosing among each corresponding recovered clock of the plurality of corresponding recovered clocks and said reference clock.

In the same field of endeavor Venkata et. al., disclose: circuitry for providing a reference clock; choosing among a plurality of clock signals

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et. al., based on the teachings of Venkata et. al., so that it

In the same field of endeavor (multiple channel communication), McCormack et. al., disclose: logic (for) selecting from the plurality of input data streams (Fig. 9, combination of muxes 513 error detector and controller (not shown), (also Fig. 10 process, column 13, lines 54-67) see column 13, lines 42-51);

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Mann et. al., based on the teachings of McCormack et. al so that data channel (receiver) settings (such as voltage level used for digitization, performed by blocks 250 in the system of Mann et. al., column 14, lines 34-36) is/are changed without loosing data (Fig. 10 of McCormack et. al, see also column 2, lines 64-67, column 3, lines 1-10).

With respect to claim 9, Mann et. al., further discloses: wherein the outgoing transmit block is a transmitter port (Fig. 7, the combiner outputs RxDAta to user interface i.e. functions as a transmitter port).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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